

**TRANSISTOR OF SEMICONDUCTOR DEVICE, AND METHOD FOR  
MANUFACTURING THE SAME**

**BACKGROUND OF THE INVENTION**

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1. Field of the Invention

The present invention relates to transistor of semiconductor device and method for manufacturing the same, and more particularly to improved transistor of memory  
10 device and method for manufacturing the same which provides a high speed and high integrated device by preventing deterioration of the characteristics of the device resulting from increase of impurity concentration as the integration of the device is increased.

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2. Description of the Background Art

As the integration of a semiconductor device has been increased, integration of a DRAM has increased. However, the refresh time of the DRAM is almost double in each generation  
20 because of a high speed and low power requirements.

As the density of a memory device continuously increases, the concentration of impurities implanted into a substrate must be increased to minimize short channel effects, threshold voltages and leakage currents. However,  
25 the increase of the concentration of impurities results in

increase of junction electric intensity, which generates short channel effects and leakage currents.

Moreover, the increase of concentration increases junction capacitance, thereby reducing the operation speed  
5 of the device.

As described above, in the conventional transistor of the semiconductor device and a method for manufacturing the same, the characteristics of the device is degraded due to the increased concentration of impurities implanted into the  
10 substrate, thereby making the achievement of the high operation speed and high integration of the semiconductor device more difficult.

#### **SUMMARY OF THE INVENTION**

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Accordingly, it is an object of the present invention to provide a transistor of a semiconductor device and a method for forming the same wherein capacitance generated by junction leakage current and junction depletion in a  
20 source/drain junction layer is removed to achieve a high speed and high integration of the device.

According to one aspect of the present invention, a transistor of a semiconductor device, comprising: an epitaxial channel region disposed on an active region of a  
25 semiconductor substrate; a stacked structure of an

insulating film and an epitaxial source/drain junction layer disposed at both sides of the channel region; and a stacked structure of a gate insulating film and a gate electrode disposed on the epitaxial channel region, wherein at least a portion of the gate insulating film overlap with the source/drain junction layer is provided.

According to another aspect of the invention, a method for forming a transistor of a semiconductor device, comprising the steps of: forming a stacked structure of a first epitaxial layer and a second epitaxial layer on a semiconductor substrate; forming a device isolation film of trench type defining an active region, wherein a thickness of the device isolation film is substantially the same as that of the stacked structure; implanting an impurity into the second epitaxial layer using the device isolation film as a mask; sequentially forming a thermal oxide film and a sacrificial film on the entire surface of the resulting structure; etching the sacrificial film, the thermal oxide film, and the second and first epitaxial layers using a gate electrode mask to form an opening exposing the semiconductor substrate; removing the first epitaxial layer to form an under-cut under the second epitaxial layer; forming an insulating film filling the under-cut; growing a third epitaxial layer on the semiconductor substrate exposed by the opening; removing the sacrificial film and the thermal

oxide film; implanting an impurity into the third epitaxial layer to form a channel region; and forming a gate electrode on the channel region is provided.

According to yet another aspect of the invention, a  
5 method for forming a transistor of a semiconductor device, comprising the steps of: forming a stacked structure of a first epitaxial layer and a second epitaxial layer on a semiconductor substrate; forming a device isolation film of trench type defining an active region; forming a dummy gate  
10 electrode on the second epitaxial layer; implanting an impurity into the second epitaxial layer using the dummy gate electrode as a mask; forming an insulating film spacer at a sidewall of the dummy gate; forming a thermal oxide film on the entire surface of the resulting structure;  
15 forming a planarized interlayer insulating film exposing the top surface of the dummy gate; etching the dummy gate and the second and first epitaxial layers therebelow to form an opening exposing the semiconductor substrate; removing the first epitaxial layer to form an under-cut under the second  
20 epitaxial layer; forming an insulating film filling the under-cut; growing a third epitaxial layer having an impurity implanted therein on the semiconductor substrate exposed by the opening; and forming a stacked structure of a gate oxide film and a gate electrode on the third epitaxial  
25 layer is provided.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become better understood  
5 with reference to the accompanying drawings which are given  
only by way of illustration and thus are not limitative of  
the present invention, wherein:

Fig. 1 is a layout diagram illustrating an active  
region and a gate region formed in one field;

10 Figs. 2a to 2f are cross-sectional diagrams  
illustrating sequential steps of a method for forming a  
transistor of a semiconductor device in accordance with a  
first embodiment of the present invention; and

Figs. 3a to 3i are cross-sectional diagrams  
15 illustrating sequential steps of a method for forming a  
transistor of a semiconductor device in accordance with a  
second embodiment of the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

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A transistor of a semiconductor device and a method  
for forming the same in accordance with preferred  
embodiments of the present invention will now be described  
in detail with reference to the accompanying drawings.

25 Fig. 1 is a layout diagram illustrating an active

region and a gate electrode region 22 formed on a semiconductor substrate 11, and Figs. 2a to 2f are cross-sectional diagrams illustrating sequential steps of a method for forming a transistor of a semiconductor device in accordance with a first embodiment of the present invention, taken along lines I-I of Fig. 1.

Referring to Fig. 2a, an first epitaxial layer 13 and a conductive second epitaxial layer 15 are sequentially formed on the semiconductor substrate 11 consisting of silicon.

Preferably, the first epitaxial layer 13 is an epitaxial SiGe layer formed under an atmosphere of a mixture gas of a gas from the group consisting of  $\text{GeH}_4$ ,  $\text{SiH}_4$ ,  $\text{SiH}_2\text{Cl}_2$  and combinations thereof,  $\text{HCl}$  and  $\text{H}_2$ , and has a thickness ranging from 50 to  $1000\text{\AA}$ , and the second epitaxial layer 15 is an epitaxial Si layer formed under an atmosphere of a gas from the group consisting of  $\text{SiH}_4$ ,  $\text{SiH}_2\text{Cl}_2$  and combinations thereof,  $\text{HCl}$  and  $\text{H}_2$ , and has a thickness ranging from 50 to  $1000\text{\AA}$ .

A pad oxide film (not shown) and a nitride film (not shown) are sequentially formed on the entire surface of the resulting structure.

Thereafter, the nitride film, the oxide film, the second epitaxial layer 15, the first epitaxial layer 13 and a predetermined depth of semiconductor substrate 11 are

etched via a photoetching process using a device isolation mask (not shown) to form a trench. A device isolation film 17 is formed by filling the trench to define an active region.

5       Next, the second epitaxial layer 15 is subjected to an implant process using the device isolation film 17 as a mask. The implant process is preferably performed using As having a concentration ranging from  $1.0E12$  to  $5.0E13$  atoms/cm<sup>2</sup> with an energy ranging from 10 to 100KeV. Other conventional  
10       impurities may be used.

      A thermal oxide film 19 is formed on the entire surface of the resulting structure. The thermal oxide film preferably has a thickness ranging from 10 to 200Å. A sacrificial film 21 is then formed on the thermal oxide film  
15       19. Preferably, the sacrificial film 21 may be an oxide film, nitride film or polysilicon film having a thickness ranging from 500 to 3000Å and used as a mask.

      Referring to Fig. 2b, a gate electrode region 22 exposing the semiconductor substrate 11 is formed by  
20       sequentially etching the sacrificial film 21, the thermal oxide film 19, the second epitaxial layer 15 and the first epitaxial layer 13 via a photoetching process using a mask exposing an region corresponding to the gate electrode region 22 of Fig. 1.

25       Referring to Fig. 2c, the first epitaxial layer 13

exposed by a lower sidewall of the gate electrode region 22 is removed to form an under-cut 23 under the second epitaxial layer 15. Preferably, the process for removing the exposed portion of the first epitaxial layer 13 is a wet  
5 etching process or an isotropic dry etching process utilizing etching selectivity differences among adjacent layers and the first epitaxial layer 13.

Specifically, the wet etching process is preferably performed using a solution containing  $H_2O$ ,  $H_2O_2$  and  $NH_4OH$   
10 having a ratio of 5 : 1 : 1 at a temperature ranging from 70 to 80°C (ref. F.S.Johnson et al. journal of electronic materials, vol21, p.805-810, 1992). The isotropic dry etching process is preferably a plasma etching process using  $HBr$ ,  $O_2$  and  $Cl_2$ , and more preferably performed using  
15 microwaves to improve isotropic etching properties. In addition, the plasma etching process may be performed using  $SF_6$ .

Now referring to Fig. 2d, an insulating film 25 for filling the under-cut 23 is formed on the entire surface of  
20 the resulting structure. Preferably, the insulating film 25 is an oxide film or nitride film.

The insulating film 25 is preferably formed via thermal oxidation, chemical vapor deposition (CVD) or atomic layer deposition (ALD).

25 Preferably, the CVD process is performed using  $SiH_4$  and



N<sub>2</sub>O under a pressure of 50Torr and at a temperature ranging from 50 to 800°C. The thermal oxidation process is a dry or wet process performed at a temperature of 700 to 1100°C.

Referring to Fig. 2e, a wet etching process is performed so that only the portion of the insulating film 25 in the under-cut 23 remains. The wet etching process is preferably performed using a HF group etching solution.

As shown in Fig. 2f, a third epitaxial layer 27 is grown on the semiconductor substrate 11 exposed by the gate electrode region 22.

Preferably, the third epitaxial layer 27 is an epitaxial Si layer having a thickness ranging from 100 to 2000Å formed under an atmosphere of a mixture gas of a gas from the group consisting of SiH<sub>4</sub>, SiH<sub>2</sub>Cl<sub>2</sub> and combinations thereof, HCl and H<sub>2</sub>.

The sacrificial oxide film 21 and the thermal oxide film 19 are removed via a wet etching process. Preferably, the wet etching process is performed by utilizing the etching selectivity difference among adjacent other layers and the sacrificial oxide film 21.

A channel region is formed on the third epitaxial layer 27 by performing a channel implant process and a punch stop implant process.

A gate electrode having a stacked structure of a gate oxide film 29, a conductive layer for gate electrode 31 and

a hard mask layer 33 is formed via a photoetching process using a gate electrode mask. Conventional conductive materials may be used as the conductive layer for gate electrode 31. The hard mask layer 33 is preferably a nitride  
5 film or an oxide film.

The formation of the channel region and removal of the sacrificial oxide film 21 and the thermal oxide film 19 may be performed prior to the formation of the gate electrode.

In the transistor of the semiconductor device formed  
10 according to the method of Figs. 2a to 2f, the conductive third epitaxial layer 27 formed in the active region of the semiconductor substrate 11 corresponds to the channel region of the transistor. The stacked structure of the insulating film 25 and the conductive second epitaxial layer 15 is  
15 formed at both sides of the third epitaxial layer 27, and the gate insulating film 29 and the gate electrode 31 are formed on the third epitaxial layer 27. The second epitaxial layer 15 corresponds to a source/drain junction layer, and at least a portion of the gate insulating film 29 overlap  
20 with the second epitaxial layer 15.

Figs. 3a to 3i are cross-sectional diagrams illustrating sequential steps of a method for forming a transistor of a semiconductor device in accordance with a second embodiment of the present invention, taken along  
25 lines I-I of Fig. 1.

Referring to Fig. 3a, an first epitaxial layer 43 and a conductive second epitaxial layer 45 are sequentially formed on the semiconductor substrate 41 comprised of silicon. Preferably, the first epitaxial layer 43 is an epitaxial SiGe layer having a thickness ranging from 50 to 1000Å formed under an atmosphere of a mixture gas of a gas from the group consisting of  $\text{GeH}_4$ ,  $\text{SiH}_4$ ,  $\text{SiH}_2\text{Cl}_2$  and combinations thereof,  $\text{HCl}$  and  $\text{H}_2$ , and the second epitaxial layer 45 is an epitaxial Si layer having a thickness ranging from 50 to 1000Å formed under an atmosphere of a mixture gas of a gas from the group consisting of  $\text{SiH}_4$ ,  $\text{SiH}_2\text{Cl}_2$  and combinations thereof,  $\text{HCl}$  and  $\text{H}_2$ .

A pad oxide film (not shown) and a nitride film (not shown) are sequentially formed on the entire surface of the resulting structure.

Thereafter, the nitride film, the oxide film, the second epitaxial layer 45, the first epitaxial layer 43 and a predetermined depth of semiconductor substrate 41 are etched via a photoetching process using a device isolation mask (not shown) to form a trench. A device isolation film 47 is formed by filling the trench to define an active region.

Referring to Fig. 3b, a polysilicon layer (not shown) is formed on the entire surface of the resulting structure, and then etched via a photoetching process using a gate

electrode mask to form a dummy gate electrode 49 in a predetermined region where a gate electrode region is to be formed. The thickness of the polysilicon layer is substantially the same as that of the gate electrode formed  
5 in a subsequent process, for example, 500 to 3000Å in thickness. An oxide film or nitride film may be used other than the polysilicon layer.

Thereafter, the second epitaxial layer 45 is subjected to an implant process using the dummy gate electrode 49 as a  
10 mask. The implant process is preferably performed using As having a concentration ranging from  $1.0E12$  to  $5.0E13$  atoms/cm<sup>2</sup> with an energy ranging from 10 to 100KeV. Other conventional impurities may be used.

The implant process may also be performed prior to the  
15 formation of the polysilicon layer using the device isolation film 47 as a mask.

Referring to Fig. 3c, an insulating film spacer 51, preferably a nitride film or an oxide film is formed at sidewalls of the dummy gate electrode 49. A thermal oxide  
20 film 53 is then formed on the entire surface of the resulting structure.

Now referring to Fig. 3d, an interlayer insulating film 55 is formed on the entire surface of the resulting structure, and then planarized to expose the top surface of  
25 the dummy gate electrode 49. Preferably, the planarization

process is a CMP process.

Referring to Fig. 3e, the exposed dummy gate electrode 49 is first removed, and the second epitaxial layer 45 and the first epitaxial layer 43 are etched using the interlayer 5 insulating film 55 and the insulating film spacer 51 as a mask to form a gate electrode region 57 exposing the semiconductor substrate 41.

Referring to Fig. 3f, the first epitaxial layer 43 exposed by a lower sidewall of the gate electrode region 57 is removed to form an under-cut 59 under the second 10 epitaxial layer 45. Preferably, the process for removing the exposed portion of the first epitaxial layer 43 is a wet etching process or an isotropic dry etching process utilizing etching selectivity differences among adjacent and 15 the first signal-crystalline layer 43.

Specifically, the wet etching process is preferably performed using a solution containing  $H_2O$ ,  $H_2O_2$ ,  $NH_4OH$  having a ratio of 5 : 1 : 1 at a temperature ranging from 70 to 80°C (ref. F.S.Johnson et al. journal of electronic 20 materials, vol21, p.805-810, 1992). The isotropic dry etching process is preferably a plasma etching process using  $HBr$ ,  $O_2$  and  $Cl_2$ , and more preferably performed using microwaves to improve isotropic etching properties. In addition, the plasma etching process may be performed using 25  $SF_6$ .

Referring to Fig. 3g, an insulating film 61 for filling the under-cut 59 is formed on the entire surface of the resulting structure. Preferably, the insulating film 61 is an oxide film or a nitride film.

5       The insulating film 61 is preferably formed via thermal oxidation, chemical vapor deposition (CVD) or atomic layer deposition (ALD).

Preferably, the CVD process is performed using  $\text{SiH}_4$  and  $\text{N}_2\text{O}$  under a pressure of 50Torr and at a temperature ranging  
10 from 50 to  $800^\circ\text{C}$ . The thermal oxidation process is a dry or wet process performed at a temperature ranging from 700 to  $1100^\circ\text{C}$ .

Referring to Fig. 3h, a wet etching process is performed so that only the portion of the insulating film 61  
15 in the under-cut 59 remains. The wet etching process is preferably performed using a HF group etching solution.

Referring to Fig. 3i, a third epitaxial layer 63, which is preferably an epitaxial Si layer having a thickness ranging from 100 to  $2000\text{\AA}$ , is grown on the semiconductor  
20 substrate 41 exposed by the gate electrode region 57.

A channel region is formed on the third epitaxial layer 63 by performing a channel implant process and a punch stop implant process.

A gate oxide film 65 is grown on the third epitaxial  
25 layer 63, and a conductive layer for gate electrode 67 is

formed on the gate oxide film 65, and then planarized using the interlayer insulating film 55 as an etch barrier to form a gate electrode.

The gate electrode may include a stacked structure of  
5 a conductive layer and a hard mask layer.

As discussed earlier, in accordance with the present invention, the transistor of the semiconductor device and the method for forming the same have the following advantages:

10 1. Generation of junction leakage current is prevented.

2. Removal of capacitance generated by junction depletion provides improved operation speed of the device.

3. Improved short channel effects/drain induced barrier lowering characteristics due to the decrease in  
15 junction depth provide decrease of a critical dimension of the gate electrode and less threshold voltage reduction.

4. The epitaxial Si layer consisting the source/drain junction region represses depletion in a bulk-wise direction to improve punch-through characteristics and allows a  
20 reduction of the dose of punch stop implant to improve refresh characteristics of the DRAM.

5. The improved punch-through characteristics allow reduction of channel threshold voltage control implant dose, thereby improving swing phenomenon and leakage current  
25 characteristics in an off state.

6. An increase in junction breakdown voltage allows a high-speed operation of the device which uses a high driving voltage.

7. A remarkable decrease in leakage current between  
5 the devices allows reduction of the depth and width of the device isolation film and achievement of high integration.

8. The epitaxial channel region and the source/drain junction region provide an improved interface characteristics of the semiconductor substrate.

10 As the present invention may be embodied in several forms without departing from the spirit or essential characteristics thereof, it should also be understood that the above-described embodiments are not limited by any of the details of the foregoing description, unless otherwise  
15 specified, but rather should be construed broadly within its spirit and scope as defined in the appended claims, and therefore all changes and modifications that fall within the metes and bounds of the claims, or equivalences of such metes and bounds are therefore intended to be embraced by  
20 the appended claims.